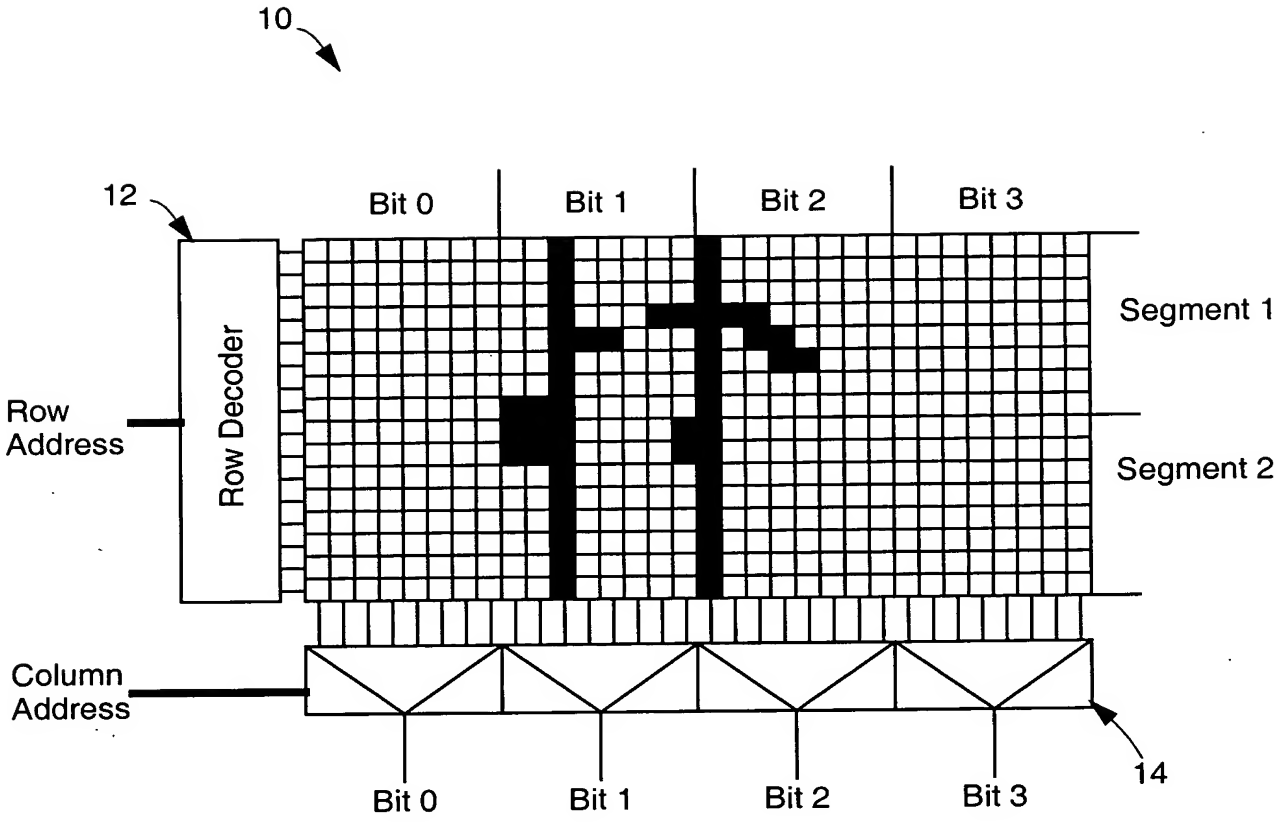


Fig. 1.
(Prior Art)

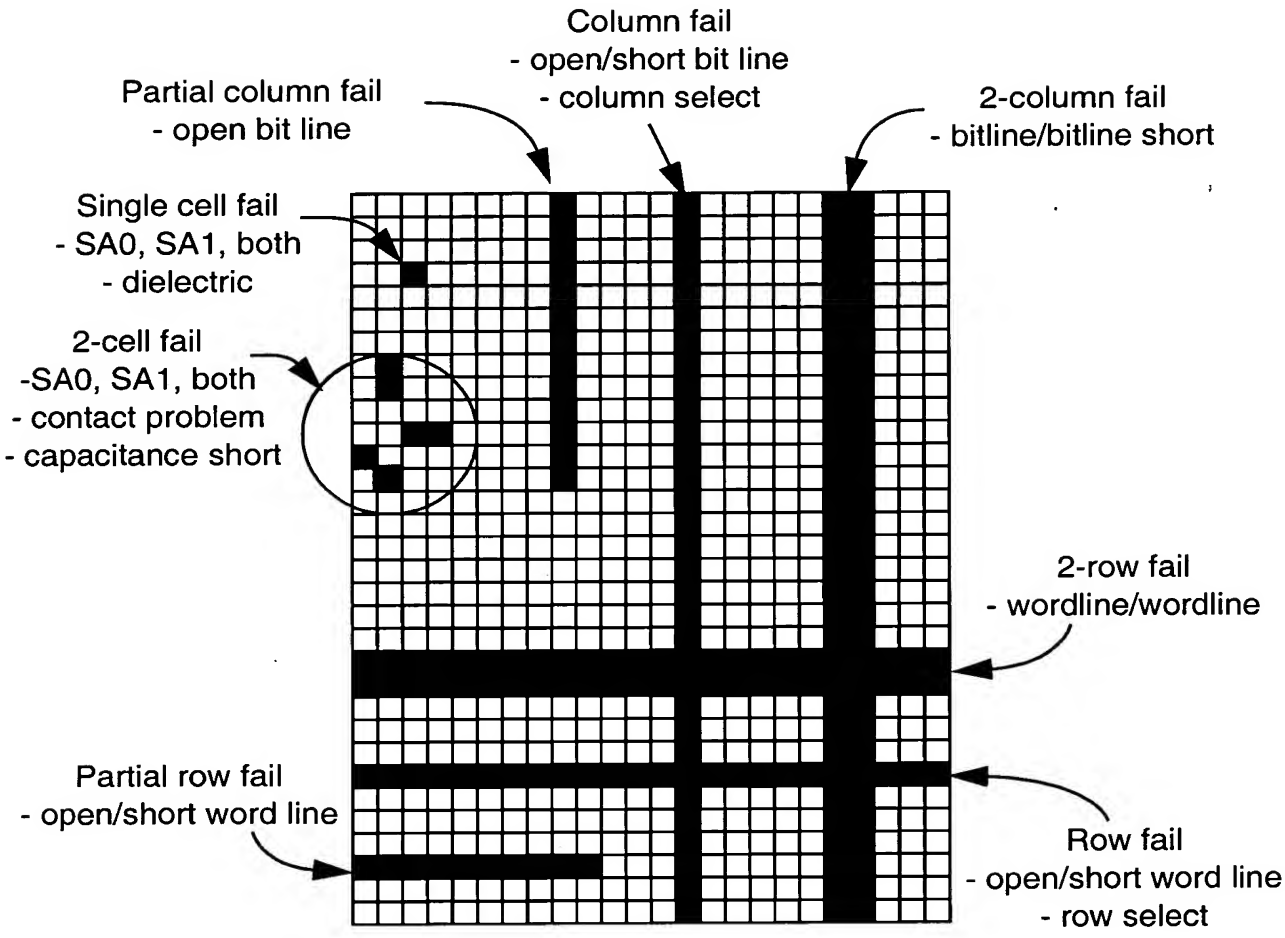


Fig. 2
(Prior Art)

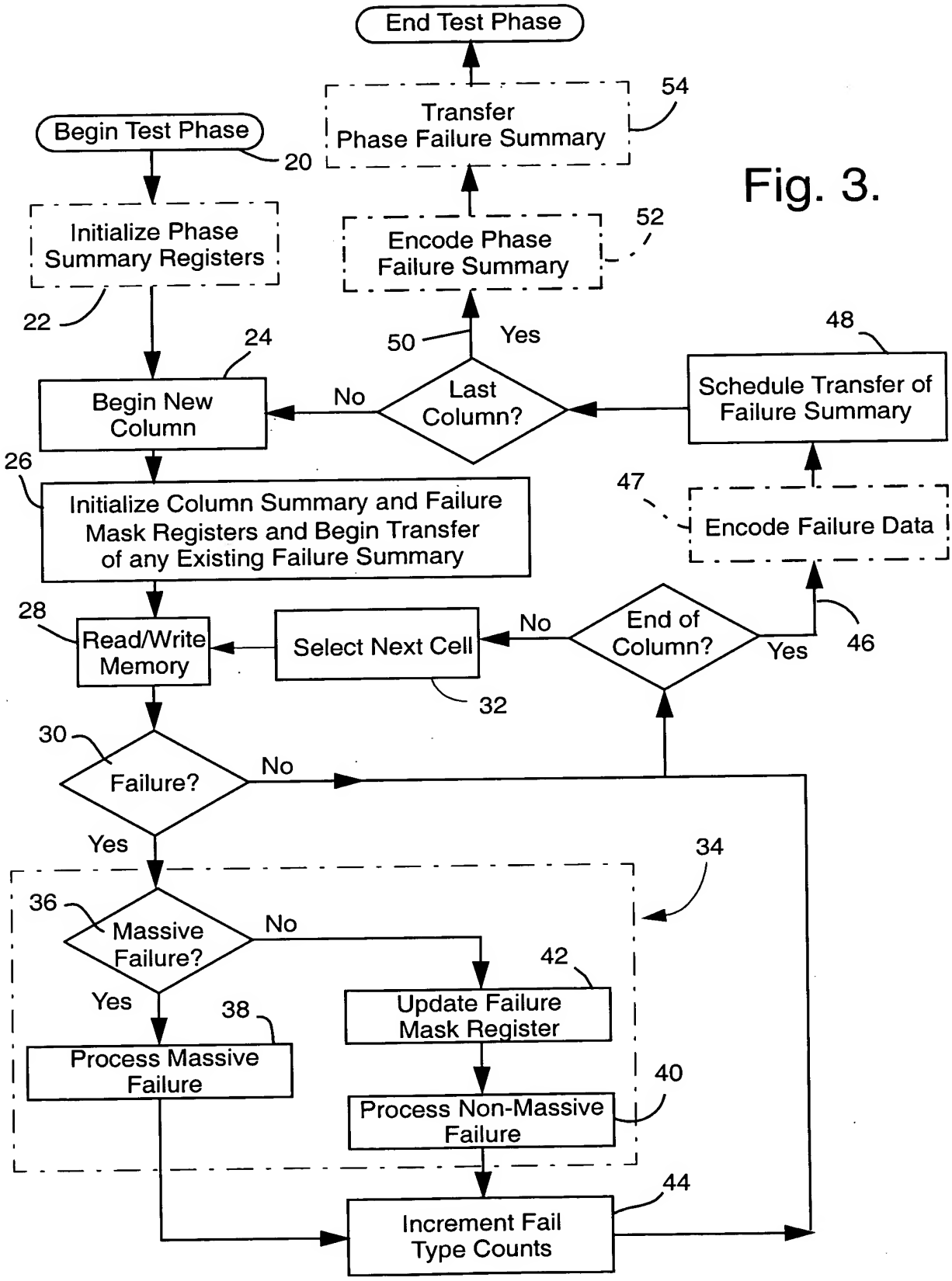

End Test Phase
54
Transfer Phase Failure Summary
Begin Test Phase
20
Initialize Phase Summary Registers
22
52
Encode Phase Failure Summary
50
Yes
48
24
Begin New Column
No
Last Column?
Schedule Transfer of Failure Summary
26
Initialize Column Summary and Failure Mask Registers and Begin Transfer of any Existing Failure Summary
47
Encode Failure Data
28
Read/Write Memory
Select Next Cell
No
End of Column?
Yes
46
32
30
Failure?
No
Yes
34
36
Massive Failure?
No
42
Update Failure Mask Register
Yes
38
Process Massive Failure
40
Process Non-Massive Failure
44
Increment Fail Type Counts

Fig. 3.

Column summary contains row addresses of first and last failure and failure counts
Row summary contains at least failure counts
Phase summary contains failure mask register information
Test is rerun for each failing bit of failure mask register

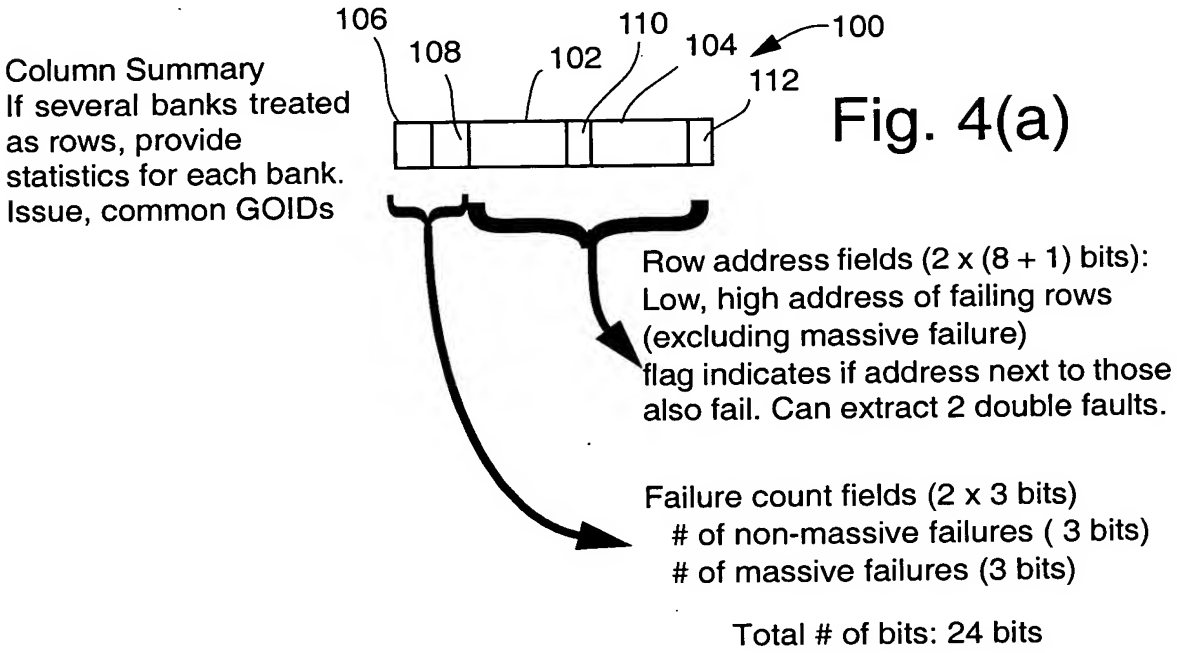


Fig. 4(a)

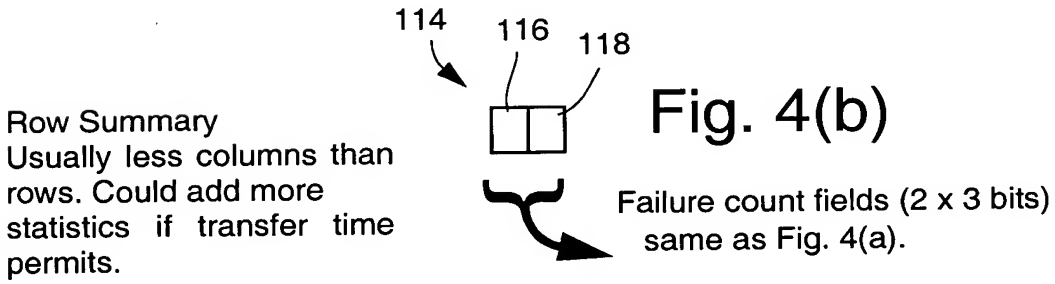


Fig. 4(b)

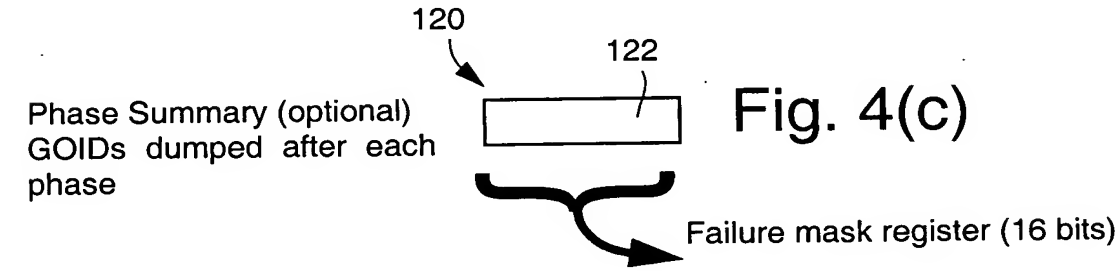


Fig. 4(c)

Column summary contains (for each of 2 address segments):
row addresses of first and last failure
failure counts: single-bit, multi-bit and massive failures
failure mask register information: number of bad bits
+Failure mask register contents for entire column: encoded for very wide memories. E.g. 64-bit word split into 8 groups of 8 bits. Only transfer register contents for 8 bits and identify group with a 3-bit field.

No row summary

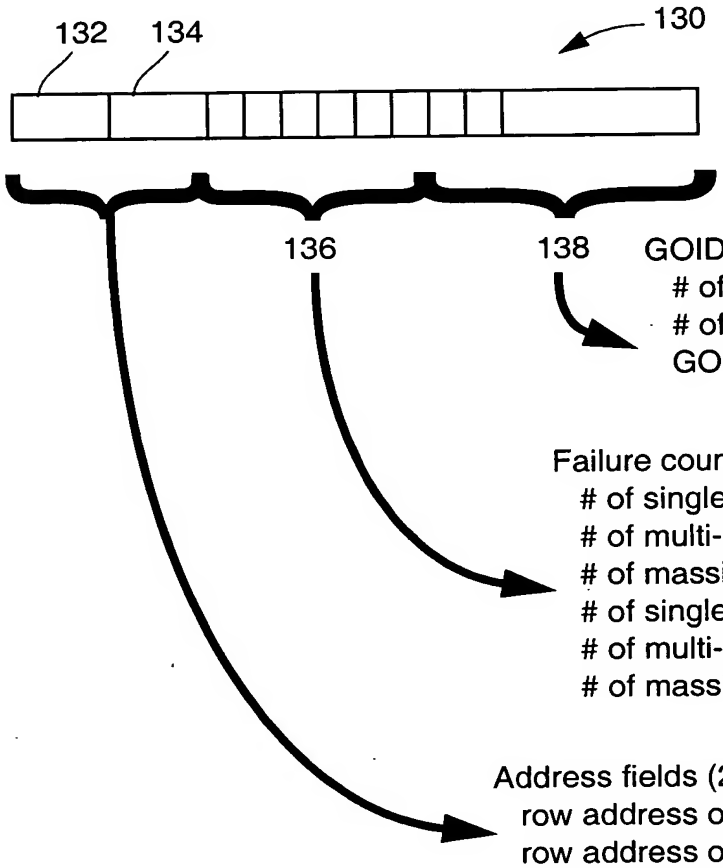


Fig. 5.

Column summary contains:

failure counts: massive and non-massive

failure mask register information: encoded or not

Row summary contains failure counts only

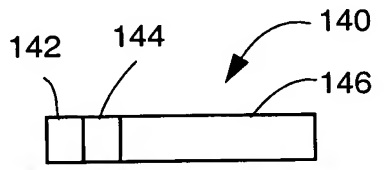


Fig. 6(a).

Column Summary

GOID fields (16 bits):
GOIDs for entire column (16 bits)
encoded or not

Failure count fields (2 x 3 bits)
# of non-massive failures (3 bits)
# of massive failures (3 bits)

Total # of bits: 22 bits

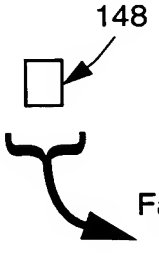


Fig. 6(b).

Row Summary

Failure count fields (1 x 3 bits)
# of failures (3 bits)

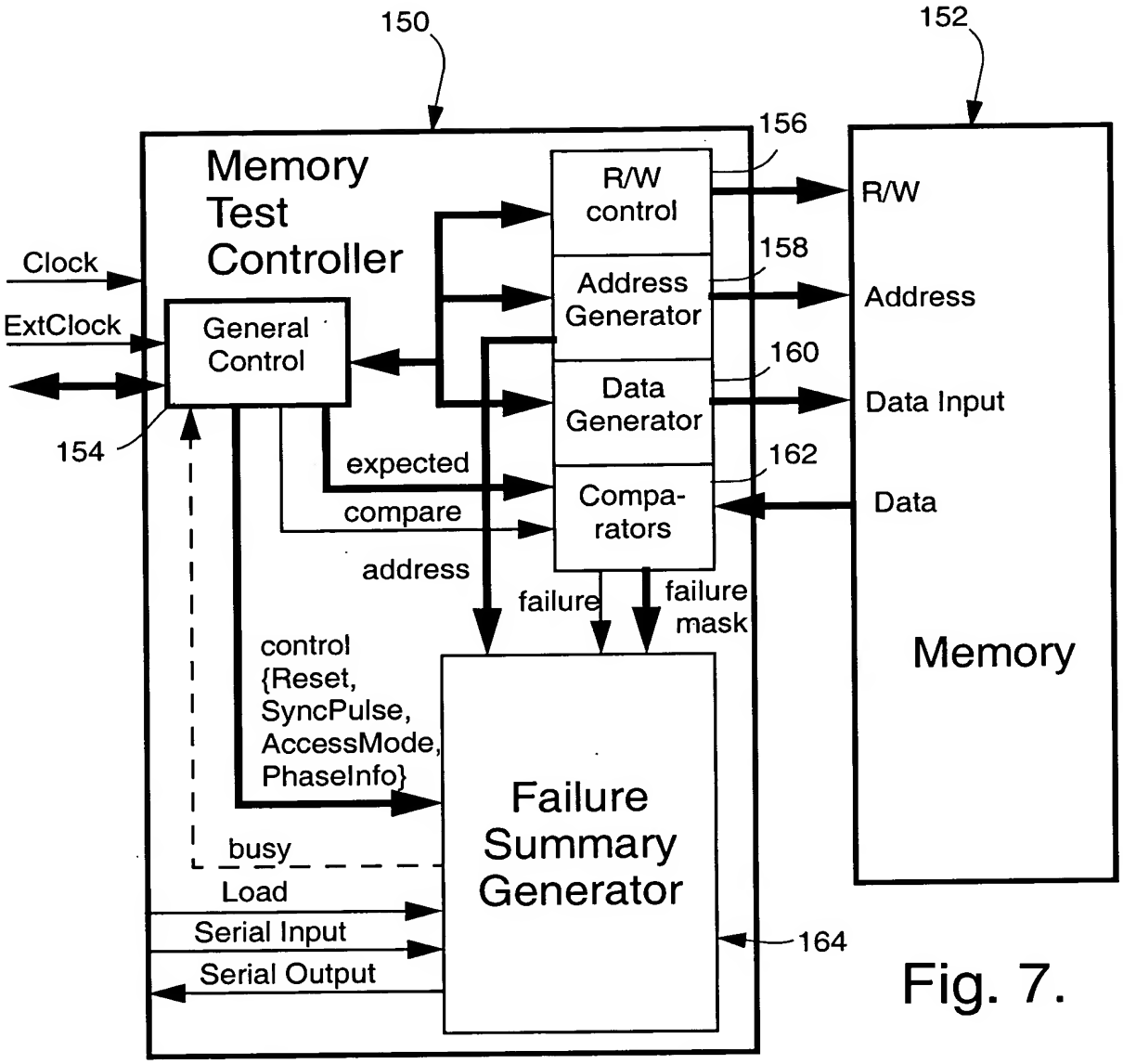
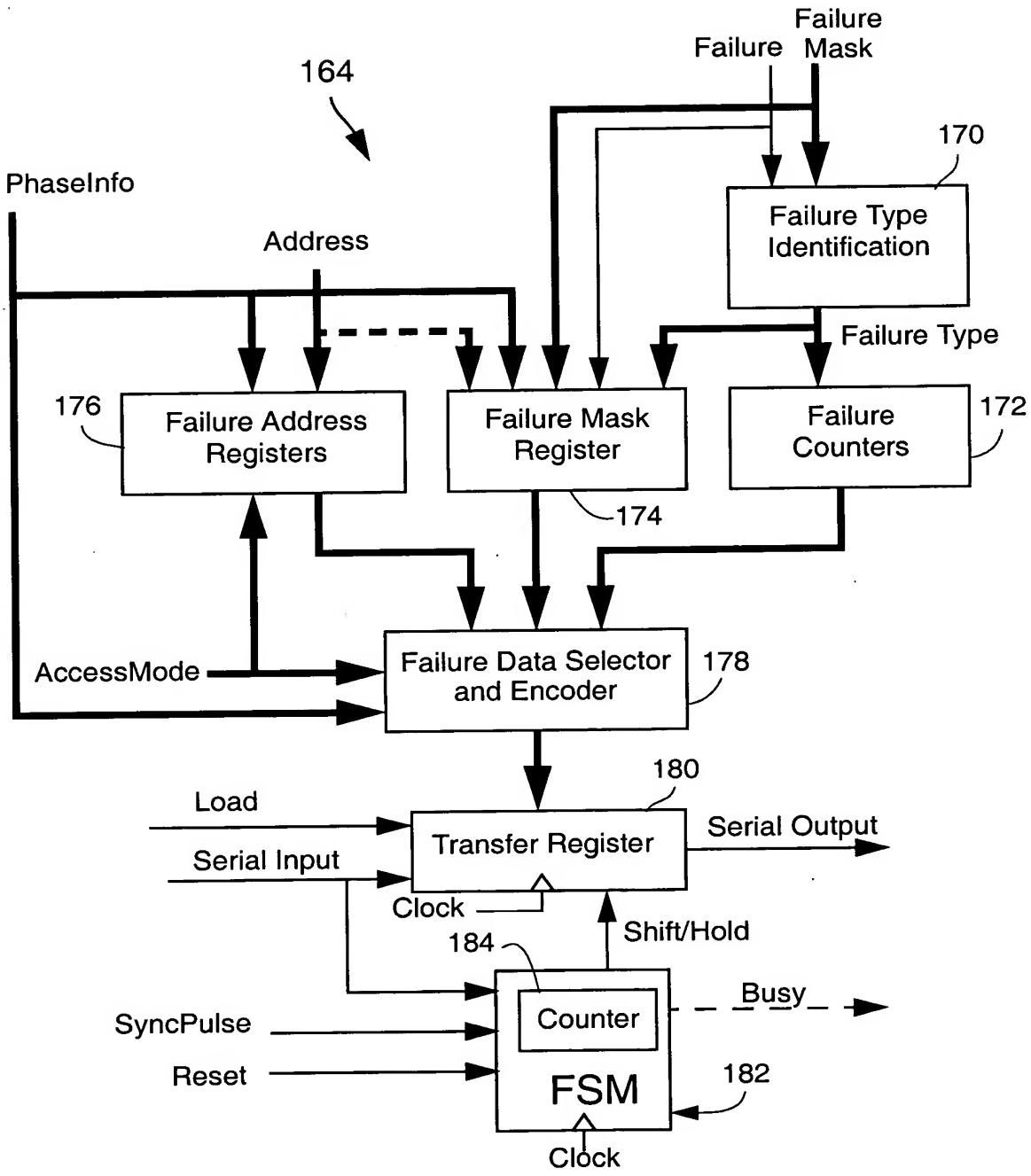

150
152
156
Memory
Test
Controller
R/W
control
R/W
Clock
158
Address
Generator
Address
ExtClock
General
Control
160
Data
Generator
Data Input
154
expected
162
Compa-
rators
Data
compare
address
failure
failure
mask
Memory
control
{Reset,
SyncPulse,
AccessMode,
PhaseInfo}
Failure
Summary
Generator
busy
Load
Serial Input
Serial Output
164

Fig. 7.

Fig. 8.


164
Failure
Failure Mask
170
PhaseInfo
Address
Failure Type Identification
Failure Type
176
Failure Address Registers
Failure Mask Register
Failure Counters
172
174
AccessMode
Failure Data Selector and Encoder
178
180
Load
Serial Input
Transfer Register
Serial Output
Clock
Shift/Hold
184
Busy
SyncPulse
Counter
Reset
FSM
182
Clock

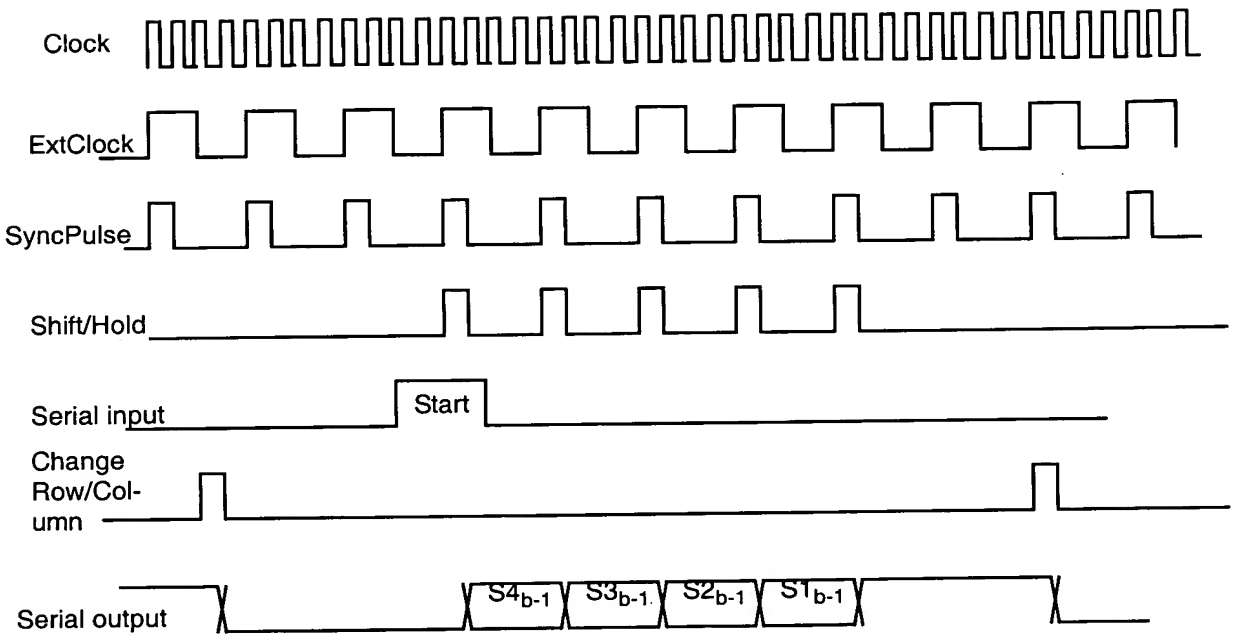

Clock
ExtClock
SyncPulse
Shift/Hold
Serial input
Start
Change Row/Col-umn
Serial output
S4b-1
S3b-1
S2b-1
S1b-1

Fig. 9.

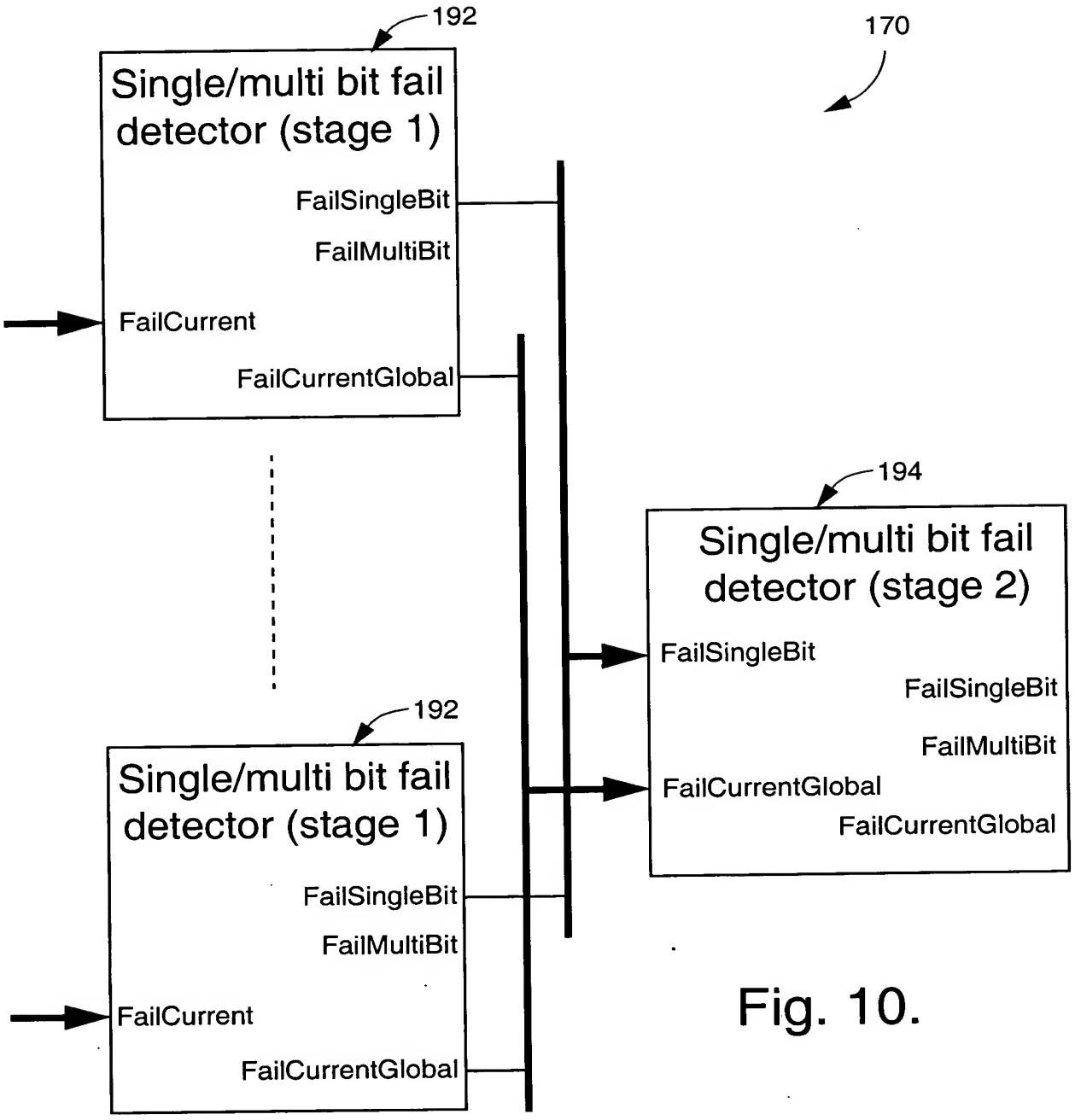

192
Single/multi bit fail detector (stage 1)
FailSingleBit
FailMultiBit
FailCurrent
FailCurrentGlobal
170
194
Single/multi bit fail detector (stage 2)
FailSingleBit
FailSingleBit
FailMultiBit
FailCurrentGlobal
FailCurrentGlobal
192
Single/multi bit fail detector (stage 1)
FailSingleBit
FailMultiBit
FailCurrent
FailCurrentGlobal

Fig. 10.

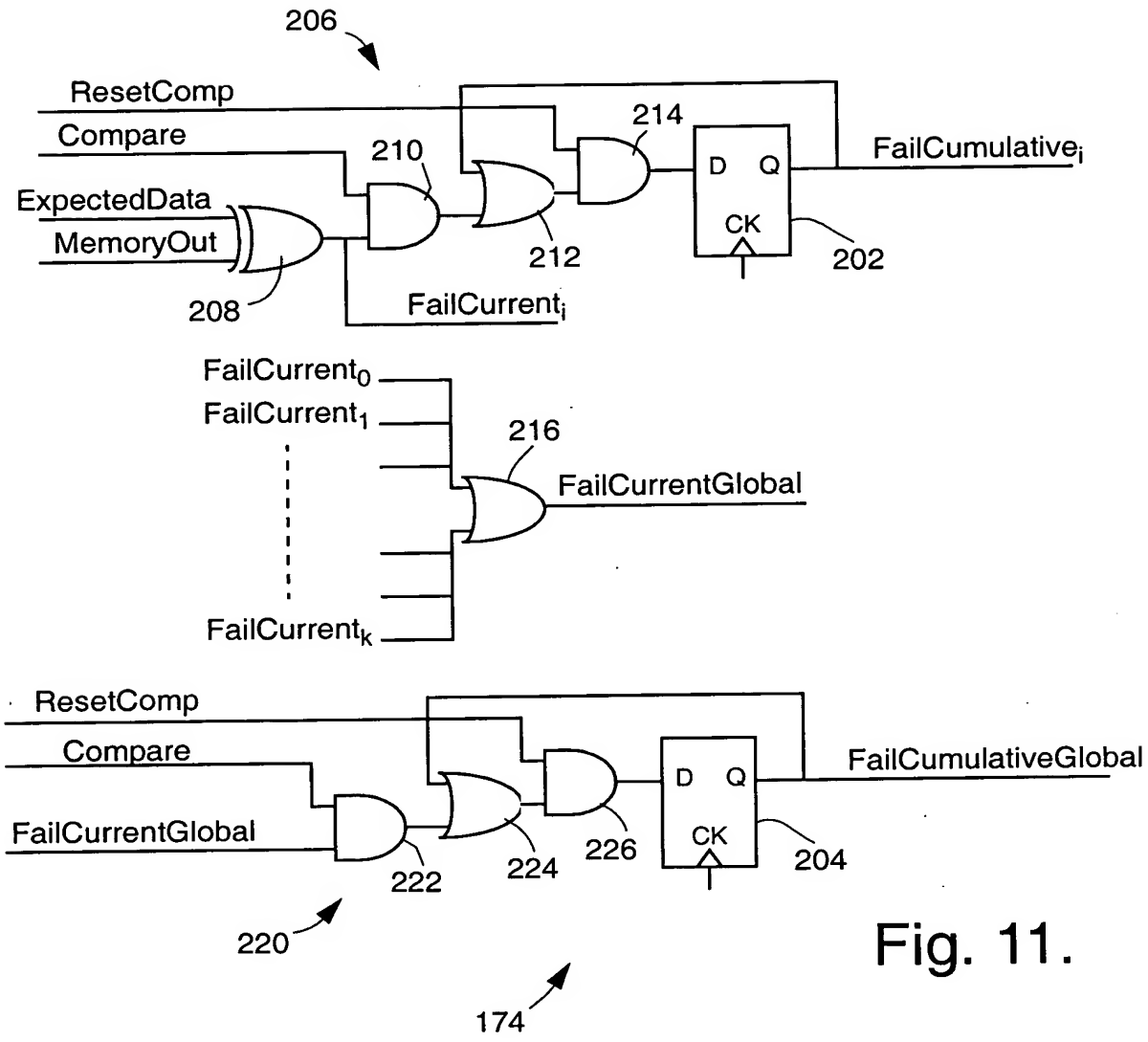

206
ResetComp
Compare
ExpectedData
MemoryOut
208
210
212
214
D
Q
CK
202
FailCumulative$_i$
FailCurrent$_i$
FailCurrent$_0$
FailCurrent$_1$
FailCurrent$_k$
216
FailCurrentGlobal
ResetComp
Compare
FailCurrentGlobal
222
224
226
D
Q
CK
204
FailCumulativeGlobal
220
174

Fig. 11.

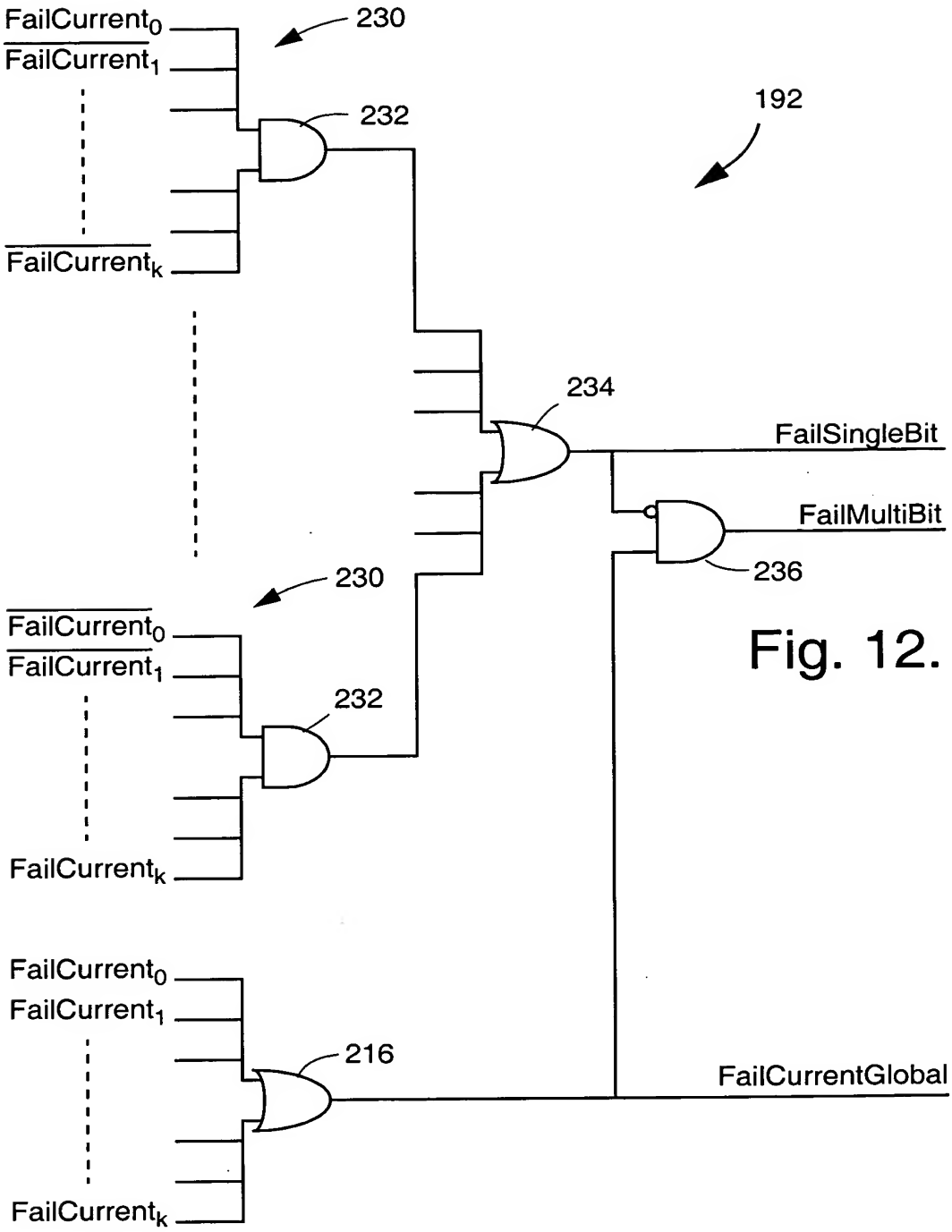

FailCurrent0
FailCurrent1
FailCurrentk
230
232
192
234
FailSingleBit
FailMultiBit
236
230
FailCurrent0
FailCurrent1
232
FailCurrentk
FailCurrent0
FailCurrent1
216
FailCurrentGlobal
FailCurrentk

Fig. 12.

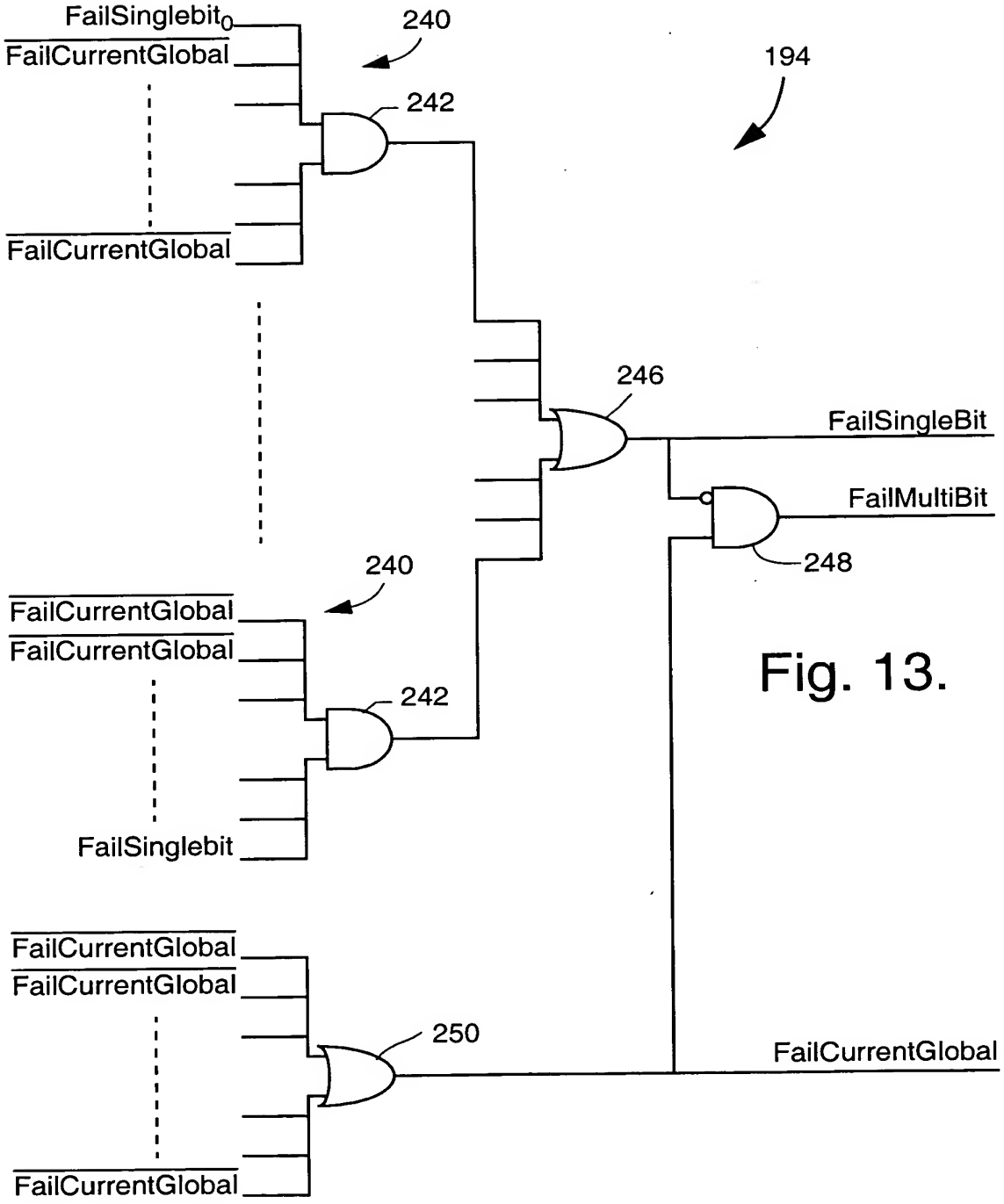

FailSinglebit0
FailCurrentGlobal
FailCurrentGlobal
240
242
194
246
FailSingleBit
FailMultiBit
248
240
FailCurrentGlobal
FailCurrentGlobal
242
FailSinglebit
FailCurrentGlobal
FailCurrentGlobal
250
FailCurrentGlobal
FailCurrentGlobal

Fig. 13.

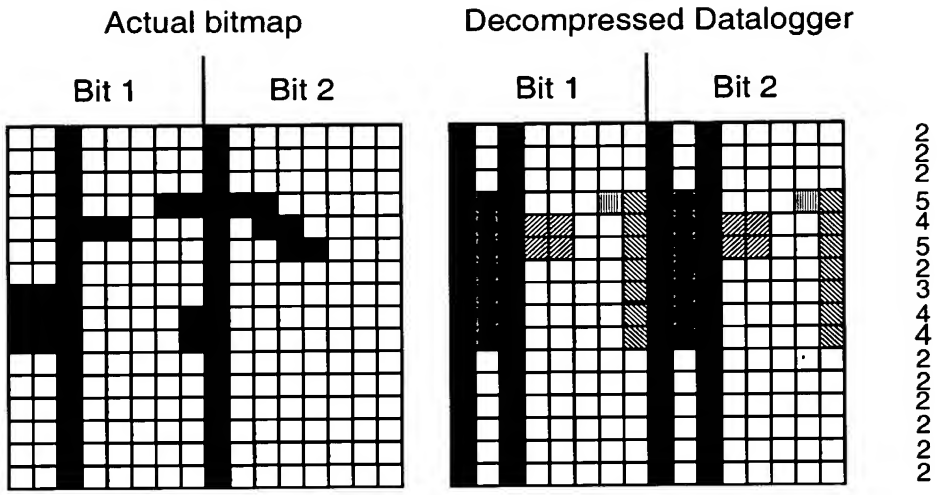
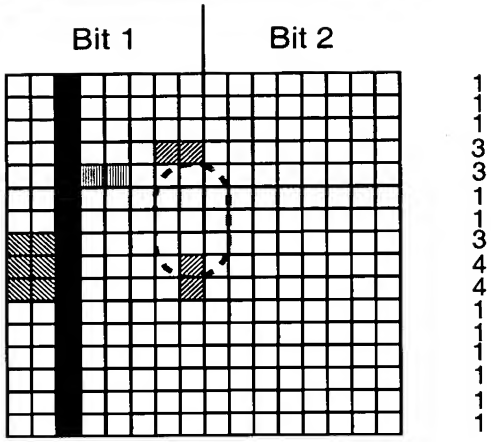


Fig. 14(a).

Pass 1

Fig. 14(b).

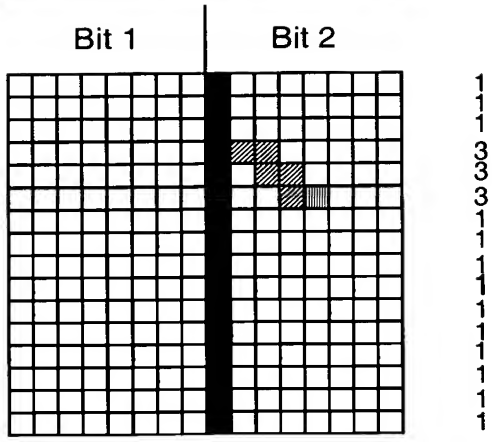
Area in dashed circled requires the row summary to resolve. All other portions only require column summary.



Pass 2, Bit 1

Fig. 14(c).

All failures for Bit 2 are resolved with the column summary



Pass 2, Bit 2

Fig. 14(d).

no fail	3< X <25% fail area	Code 4
1 fail area	25%< X <50% fail area	Code 5
2 fail area	50%< X <100% fail area	Code 6
3 fail area	100% fail area	Code 7

X - No. of Failures

Column Number	Pass 1	Pass 2 Bit 1	Pass 2 Bit 2
0	7 0 00 1 FF 1	3 0 07 1 09 1	7 0 00 1 FF 1
1	4 0 03 0 09 1	3 0 07 1 09 1	1 0 03 0 03 0
2	7 0 00 1 FF 1	7 0 00 1 FF 1	2 0 03 1 04 1
3	2 0 04 1 05 1	1 0 04 0 04 0	2 0 04 1 05 1
4	2 0 04 1 05 1	1 0 04 0 04 0	1 0 05 0 05 0
5	0 0 00 0 00 0	0 0 00 0 00 0	0 0 00 0 00 0
6	1 0 03 0 03 0	1 0 03 0 03 0	0 0 00 0 00 0
7	3 0 03 0 09 1	3 0 03 0 09 1	0 0 00 0 00 0

Fig. 14(e)

Pass 1	Pass 2 Bit 1	Pass 2 Bit 2
0110000000000000	0100000000000000	0010000000000000

Fig. 14(f)